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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

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Method of Forming Trench Isolation Regions

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ATTORNEY'S DOCKET NO. MI22-1198

TECHNICAL FIELD

This invention relates to methods of forming trench isolation regions in semiconductive substrates.

BACKGROUND OF THE INVENTION

In modern semiconductor device applications, numerous devices are packed onto a single small area of a semiconductor substrate to create an integrated circuit. For the circuit to function, many of these individual devices may need to be electrically isolated from one another. Accordingly, electrical isolation is an important and integral part of semiconductor device design for preventing the unwanted electrical coupling between adjacent components and devices.

As the size of integrated circuits is reduced, the devices that make up the circuits must be positioned closer together in order to comply with the limited space available on a typical semiconductor substrate. As the industry strives towards a greater density of active components per unit area of semiconductor substrate, effective isolation between circuits becomes all the more important.

The conventional method of isolating circuit components in modern integrated circuit technology takes the form of trench isolation regions etched into a semiconductor substrate. Trench isolation regions are commonly divided into three categories: shallow trenches (STI) (trenches less than about 1 micron deep); moderate depth trenches (trenches of

1 from about 1 to about 3 microns deep); and deep trenches (trenches
2 greater than about 3 microns deep). Once the trench isolation regions
3 are etched in the semiconductor substrate, a dielectric material is
4 deposited to fill the trenches. As the density of components on the
5 semiconductor substrate increased, the widths of the trenches decreased
6 until the process of flowing dielectric material into the trenches
7 developed problems.

8 Trench isolation regions, particularly STI regions, can develop
9 undesirable voids in the dielectric material during the process to fill the
10 trenches. As the dielectric material flows to an edge between a
11 substrate surface and a sidewall of the trench, constrictions develop at
12 the top of trenches due to the narrow opening in the trench. As the
13 dielectric material flows into the trench, the constrictions can develop
14 into voids moving into the trench with the dielectric material. Voids
15 lower the dielectric characteristics of the dielectric material used and
16 introduce structural instabilities in subsequent processes. Accordingly,
17 voids in the dielectric material filling an isolation trench region are
18 highly undesirable.

19 20 SUMMARY OF THE INVENTION

21 In accordance with an aspect of the invention, a method of
22 forming a trench isolation region includes forming a trench within a
23 substrate. A silanol layer is formed to partially fill the trench and

1 then at least some of the silanol is converted to a compound comprising
2 at least one of SiO_n and RSiO_n , where R comprises an organic group.
3 An electrically insulative material is formed over the converted silanol to
4 fill the trench.

5 In another aspect of the invention, a method of forming a trench
6 isolation region includes forming a trench within a substrate. A first
7 layer of at least one of Si(OH)_x and $(\text{CH}_3)_y\text{Si(OH)}_{4-y}$ is formed to
8 partially fill the trench. At least some of the Si(OH)_x if present is
9 converted to SiO_2 and at least some of $(\text{CH}_3)_y\text{Si(OH)}_{4-y}$ if present is
10 converted to $(\text{CH}_3)_x\text{SiO}_{2-x}$. Next, a layer of an electrically insulative
11 material is formed to fill the trench.

12 In yet another aspect of the invention, a method of forming a
13 trench isolation region includes forming a trench within a substrate. The
14 trench has sidewalls comprising silicon and a base comprising silicon.
15 A first electrically insulative layer is formed over the sidewalls and base.
16 The first electrically insulative layer is anisotropically etched to expose
17 silicon of the base while leaving silicon of the sidewalls covered. A
18 second electrically insulative layer is substantially selectively chemical
19 vapor deposited over the exposed trench base. A third electrically
20 insulative layer is formed over the first and second insulative layers to
21 within the trench.

22 In still another aspect of the invention, a method of forming a
23 trench isolation region includes forming a trench having sidewalls within

1 a substrate. The sidewalls are thermally oxidized in an oxidizing
2 environment which includes oxygen and hydrogen with a greater molar
3 concentration of hydrogen than oxygen. A layer of silanol is formed to
4 within the trench and at least some of the silanol is converted to a
5 compound of at least one of SiO_n and RSiO_n , where R includes an
6 organic group.

7 8 BRIEF DESCRIPTION OF THE DRAWINGS

9 Preferred embodiments of the invention are described below with
10 reference to the following accompanying drawings.

11 Figure 1 is a fragmentary sectional view of a semiconductor
12 substrate at one processing step in accordance with a first embodiment
13 of the invention.

14 Figure 2 is a view of the Figure 1 substrate fragment at a
15 processing step subsequent to that shown in Figure 1.

16 Figure 3 is a view of the Figure 1 substrate fragment at a
17 processing step subsequent to that shown in of Figure 2.

18 Figure 4 is a view of the Figure 1 substrate fragment at a
19 processing step subsequent to that shown in of Figure 3.

20 Figure 5 is a fragmentary sectional view of a semiconductor
21 substrate at one processing step in accordance with a second embodiment
22 of the invention.
23

1 Figure 6 is a view of the Figure 5 substrate fragment at a
2 processing step subsequent to that of Figure 5.

3 Figure 7 is a view of the Figure 5 substrate fragment at a
4 processing step subsequent to that of Figure 6.

5 Figure 8 is a fragmentary sectional view of a semiconductor
6 substrate at one processing step in accordance with a third embodiment
7 of the invention.

8 Figure 9 is a view of the Figure 8 substrate fragment at a
9 processing step subsequent to that of Figure 8.

10 Figure 10 is a view of the Figure 8 substrate fragment at a
11 processing step subsequent to that of Figure 9.

12 Figure 11 is a view of the Figure 8 substrate fragment at a
13 processing step subsequent to that of Figure 10.

14 Figure 12 is a view of the Figure 8 substrate fragment at a
15 processing step subsequent to that of Figure 11.

16 Figure 13 is a fragmentary sectional view of a semiconductor
17 substrate at one processing step in accordance with a fourth embodiment
18 of the invention.

19 Figure 14 is a view of the Figure 13 substrate fragment at a
20 processing step subsequent to that of Figure 13.

21 Figure 15 is a view of the Figure 13 substrate fragment at a
22 processing step subsequent to that of Figure 14.
23

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

With reference to Figures 1-4, a method of forming a trench isolation region is illustrated. Referring to Figure 1, a semiconductor substrate fragment in process is indicated generally with reference numeral 10. Preferably, the semiconductor substrate fragment 10 comprises the following layers shown in elevationally ascending order: a semiconductor substrate 12, preferably a bulk monocrystalline silicon substrate; an oxide layer 20; and a silicon nitride layer 22. A series of trenches 14 are formed, preferably by an etching process, through layers 20 and 22 and within semiconductor substrate 12. Trench isolation regions 14 have sidewalls 16 and base walls 18.

Referring to Figure 2, a first layer 26 is formed, and initially comprises a silanol which partially fills trenches 14. An exemplary method of forming the first layer 26 is as follows. SiH_4 and H_2O_2 are separately introduced into a chemical vapor deposition (CVD) chamber, such as a parallel plate reaction chamber (not shown). The reaction rate between SiH_4 and H_2O_2 can be moderated by the introduction of nitrogen into the reaction chamber. Semiconductive substrate 12 within the chamber is preferably maintained at a suitably low temperature, such as 0°C , at an exemplary pressure of 1 Torr to achieve formation of a

1 silanol-type material of the formula Si(OH)_x , which is predominately
2 Si(OH)_4 . The Si(OH)_4 condenses onto the semiconductor substrate 12
3 surface to form layer 26.

4 Alternatively, first layer 26 is formed to comprise $(\text{CH}_3)_y\text{Si(OH)}_{4-y}$
5 at least initially to partially fill the trench. The formation of
6 $(\text{CH}_3)_y\text{Si(OH)}_{4-y}$ can be accomplished similarly to that described above for
7 forming silanol, with the exception that $(\text{CH}_3)_z\text{SiH}_{4-z}$, wherein z is at
8 least 1 and no greater than 4, is combined with the hydrogen peroxide
9 (H_2O_2). For example, CH_3SiH_3 can be combined with H_2O_2 to produce
10 $\text{CH}_3\text{Si(OH)}_3$.

11 Although either reaction occurs in the gas phase, the initially
12 deposited first layer 26 (Si(OH)_x or $(\text{CH}_3)_y\text{Si(OH)}_{4-y}$) is preferably in the
13 form of a viscous liquid which preferably flows very conformably, ideally
14 depositing over trench base 18 faster and thicker than over sidewalls 16.
15 A preferred thickness for first layer 26 is at least 25% of the trench
16 depth, and more preferably at least 35%, while preferably adding
17 only 200 angstroms or less to sidewalls 16.

18 After forming first layer 26 over semiconductor substrate 12, at
19 least some of it is converted to a compound comprising at least one of
20 SiO_n and RSiO_n , where R comprises an organic group. An exemplary
21 process for doing so is to treat first layer 26 with energy to drive water
22 therefrom and convert to a silicon oxide comprising structure. A specific
23 exemplary method of converting first layer 26 comprises exposing the first

1 layer 26 to ultraviolet light, with other examples of energy being electron
2 beam energy or plasma, and RF energy. Preferably, a two-step process
3 is employed. First, polymerization of the liquid film is promoted by
4 increasing the temperature to above 100°C, while maintaining the
5 pressure of about 1 Torr, to result in solidification and formation of a
6 polymer layer. Thereafter, the temperature is raised to above 300°C,
7 preferably above 400°C, while maintaining a pressure of about 1 Torr,
8 preferably at least 10 atmospheres.

9 Referring to Figure 3, a second layer 30 is formed comprising an
10 electrically insulative material, preferably silicon dioxide, over converted
11 silanol layer 26 to within the trenches 14. Preferably as shown, second
12 layer 30 is formed to fill remaining volume of trenches 14. An
13 exemplary process for forming second layer 30 comprises chemical vapor
14 deposition, preferably plasma-enhanced chemical vapor deposition. For
15 example, conventional high density plasma deposited SiO_2 can be formed.
16 In the context of this document, "high density" refers to a plasma
17 having at least 10^{10} ions/cm³ plasma density. An optional gettering
18 process may be performed at this stage of the process.

19 Referring to Figure 4, planarization can be conducted (i.e.,
20 chemical-mechanical polishing) to remove layers 30, 22 and 20 from over
21 the substrate outside of trenches 14.

22 With reference to Figures 5-7, another embodiment in accordance
23 with the invention is described. Like numerals from the first described

embodiment are employed where appropriate, with differences being indicated with a suffix (a) or with different numerals.

Referring to Figure 5, a semiconductor substrate fragment in process is indicated generally with reference numeral 10a. An electrically insulating first layer 40 is chemical vapor deposited to within trenches 14 to partially fill the trenches. Preferably, first layer 40 comprises silicon dioxide (SiO_2) and fills at least 25% of the trench 14 depth. First layer 40 is preferably deposited by plasma-enhanced chemical vapor deposition, preferably by high density plasma or subatmospheric chemical vapor deposition.

Referring to Figure 6, a second layer 44 comprising a silanol is formed over first layer 40 to within trenches 14. Preferably, the method to form second layer 44 is by the same method previously discussed and disclosed for forming first layer 26 of the Figures 1-4 embodiment. Consequently, as with the previous method, second layer 44 preferably fills trenches 14, preferably is maintained at a temperature of at least about 300° C and at a pressure of at least about 10 atmospheres effective to drive water from second layer 44, and preferably is converted to a silicon oxide comprising structure by exposure to energy, for example ultraviolet light.

Referring to Figure 7, planarization can be conducted (i.e., chemical-mechanical polishing) to remove layers 44, 40, 22 and 20 from over the substrate outside of trenches 14.

1 With reference to Figures 8-12, yet another embodiment in
2 accordance with the invention is described. Like numerals from the
3 previously described embodiments are employed where appropriate, with
4 differences being indicated with a suffix (b) or with different numerals.

5 Referring to Figure 8, a semiconductor substrate fragment in
6 process is indicated generally with reference numeral 10b. An
7 electrically insulative layer 21 is formed over silicon trench sidewalls 16
8 and trench base 18. An example thickness for layer 21 is 150
9 angstroms. A preferred material for layer 21 is silicon dioxide. An
10 exemplary method of forming layer 21 comprises chemical vapor
11 deposition, and alternatively thermal oxidation. An example thermal
12 oxidation comprises flowing an oxidizing gas (i.e., O_2 , O_3 , N_2O , NO_x or
13 any mixture combination thereof) over substrate 12 within trenches 14
14 while substrate 12 is maintained at from 850°C to 1150°C for from 5
15 to 30 minutes. An example chemical vapor deposition process comprises
16 injecting tetraethylorthosilicate (TEOS) into a reactor chamber at 500
17 mg/min while flowing O_3 , preferably as a mixture of 12% O_3 and 88%
18 O_2 , at 4000 sccm and helium at from 0-200 sccm and maintaining the
19 substrate 12 at 550°C and reactor pressure at 200 Torr.

20 Referring to Figure 9, insulative layer 21 is anisotropically etched
21 to expose silicon of the base walls 18 while leaving silicon of the
22 sidewalls 16 covered. An exemplary anisotropic etch comprises a
23 conventional oxide spacer etch.

1 Referring to Figure 10, a second electrically insulative layer 50 is
2 substantially selectively deposited over the exposed base walls 18 to
3 partially fill the trenches 14. Preferably, layer 50 comprises an oxide
4 deposited by chemical vapor deposition, and more preferably silicon
5 dioxide. An exemplary chemical vapor deposition to form layer 50
6 comprises liquid injecting TEOS into a reactor chamber at 350 mg/min
7 while flowing O₃, preferably as a mixture of 12% O₃ and 88% O₂,
8 at 5000 sccm and helium at from 0-200 sccm and maintaining the
9 substrate 12 at 400°C and reactor pressure at 600 Torr.

10 Referring to Figure 11, a layer 30 is formed comprising an
11 electrically insulative material, preferably silicon dioxide, over
12 layers 21, 22 and 50 to within trenches 14. Preferably as shown,
13 layer 30 is formed to fill remaining volume of trenches 14. An
14 exemplary process for forming second layer 30 comprises chemical vapor
15 deposition, preferably high density plasma-enhanced chemical vapor
16 deposition as described above. An alternative method of forming
17 layer 30 comprises flowing a silanol layer to fill within trenches 14. The
18 method to form layer 30 is preferably by the same method previously
19 discussed and disclosed for forming first layer 26 of the first embodiment
20 shown in Figures 1-4 and second layer 44 of the second embodiment
21 shown in Figures 5-7.
22
23

1 Referring to Figure 12, planarization can be conducted (i.e.,
2 chemical-mechanical polishing) to remove layers 30, 22, 21 and 20 from
3 over substrate 12 outside of trenches 14.

4 With reference to Figures 13-15, still another embodiment in
5 accordance with the invention is described. Like numerals from the first
6 described embodiment are employed where appropriate, with differences
7 being indicated with a suffix (c) or with different numerals. Referring
8 to Figure 13, an electrically insulative layer 21 is formed over silicon
9 trench sidewalls 16 and trench base 18 by a thermal oxidization process.
10 An exemplary method of forming layer 21 comprises thermally oxidizing
11 the sidewalls of the trench in an oxidizing environment comprising oxygen
12 and hydrogen and having a greater molar concentration of hydrogen than
13 oxygen. An example thermal oxidation comprises flowing an oxidizing
14 gas at 200 sccm (i.e., O_2 , O_3 , N_2O , NO_x or any mixture combination
15 thereof) and hydrogen source at 1 slm (i.e., H_2 , NH_3 or any mixture
16 combination thereof) over substrate 12 within trenches 14. Preferably,
17 substrate 12 is maintained at from 800°C to 1100°C and reactor pressure
18 at from 10 Torr to 760 Torr for from 1 to 20 minutes.

19 Referring to Figure 14, a silanol layer 44 is formed over layers 21
20 and 22 to within trenches 14. At least some of the silanol is converted
21 to a compound comprising at least one of SiO_n and $RSiO_n$, where R
22 comprises an organic group. The method to form layer 44 is preferably
23 by the same method previously discussed and disclosed for forming first

1 layer 26 of the first embodiment shown in Figures 1-4 and second
2 layer 44 of the second embodiment shown in Figures 5-7.

3 Referring to Figure 15, planarization can be conducted (i.e.,
4 chemical-mechanical polishing) to remove layers 44, 22, 21 and 20 from
5 over substrate 12 outside of trenches 14.

6 Alternatively, the silanol 44 could be formed within trenches 14
7 and converted before a sidewall oxidation. Preferably in such instance,
8 the thermal oxidation conditions comprise flowing an oxidizing gas at 200
9 sccm (i.e., O_2 , O_3 , N_2O , NO_x or any mixture combination thereof) over
10 substrate 12 within trenches 14 while substrate 12 is maintained at
11 from 850°C to 1150°C and reactor pressure at from 10 Torr to 760 Torr
12 for from 5 to 30 minutes.

13 Further in accordance with the invention, sidewalls 16 might be
14 oxidized prior to forming first layer 26 in the first embodiment, or prior
15 to forming first layer 40 in the second embodiment. Alternately,
16 sidewalls 16 might be oxidized after forming first layer 26 and before
17 forming second layer 30 in the first embodiment, or after forming first
18 layer 40 and before forming second layer 44 in the second embodiment
19 or after forming layer 50 and before forming layer 30 in the third
20 embodiment. Further alternately, sidewalls 16 might be oxidized after
21 forming second layer 30 in the first embodiment, or after forming
22 layer 44 in the second embodiment. Further alternately with respect to
23 the third embodiment, and where layer 21 is not formed by thermal

1 oxidation, the sidewalls might be oxidized after forming layer 50 and
2 before forming layer 30, or after forming layer 50. Conventional thermal
3 oxidations are preferably conducted in such instances.

4 In the preferred first embodiment, first layer 26 flows conformably
5 into the trenches during deposition without forming any constrictions at
6 the top of the trenches where voids begin. The first layer 26 effectively
7 lowers the aspect ratio (defined as trench depth to width) of the
8 trenches preferably by filling at least about a third of the depth while
9 only adding at most 200 angstroms of layer on the sidewalls. As a
10 result, any subsequent layer deposited to fill the layer will have a trench
11 with a lower aspect ratio more conducive to filling without voids.

12 In the less preferred second and third embodiments, the first layer
13 is formed by less preferred methods which may not lower the aspect
14 ratio as significantly as in the first embodiment.

15 In compliance with the statute, the invention has been described
16 in language more or less specific as to structural and methodical
17 features. It is to be understood, however, that the invention is not
18 limited to the specific features shown and described, since the means
19 herein disclosed comprise preferred forms of putting the invention into
20 effect. The invention is, therefore, claimed in any of its forms or
21 modifications within the proper scope of the appended claims
22 appropriately interpreted in accordance with the doctrine of equivalents.
23